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PETERS
Speziallacke für die Elektronik

TI TECHNICAL INFORMATION

Plugging processes – Filling of buried vias by means of the plugging process –

TI 15/15

This Technical Information sheet provides recommendations on the use of plugging pastes for the manufacture of High Density Interconnect (HDI) circuits.

Application fields are defined as well as various plugging materials and processing possibilities presented.

Not even the most important German work of reference, "Grosser" Brockhaus, the Brockhaus Encyclopedia (30 volumes), defines the term "Loch“ (German for "hole"). The keyword "hole" merely offers the following definition:
Hole: Scottish-Gaelic, Irish-Gaelic, Anglicized in Ireland Lough, lake, bay, Loch Ness, for instance.

Therefore please find below three definitions on the subject of "Loch“ by Kurt Tucholski, a German author, 1890 – 1935:

1. *"A hole is there where nothing exists.“*
2. *"A hole is a permanent companion of the non-hole.“*
3. *"If man sees a hole he intends to fill it. While doing so, he often falls into it.“*

In order to prevent our customers from falling into the hole when "filling holes" by means of plugging pastes we have compiled this **Technical Information sheet TI 15/15**, because "the European Technology and trend report 2001/2002 on high density interconnected pwbs (HDI)“ and also the "DVS/GMM pcb specialist conference of February 6 and 7, 2002 in Fellbach“ have clearly shown that HDI technology is becoming more and more important. The plugging process, i.e. the filling of the holes, plays a key role in this process.

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1. General information

Owing to the increasing use of High Density Interconnect PWB's (HDI pwbs), the plugging of microvias has become an inevitable subject for many manufacturers of printed circuit boards. It becomes obvious that the plugging of vias has its "vagaries". Starting with all the most different types of vias, the various requirements on the filling materials, the different application processes right through to the required post-treatments - numerous questions arise.

This technical information sheet defines commonly used terms around the topic of via hole fillers and explains the various application fields of via hole fillers and their requirements.

The next special subject is plugging. Various materials, applications and process steps are presented.

Last but not least, this TI shall assist in finding the right process for the plugging of microvias in order to realize a low-cost and high-quality production of HDI pwbs.

2. Definition

The term "plugging" (filling, closing) that is meanwhile internationally interpreted as the planar filling of buried vias, has become one of the key processes in microvia technology. In order to properly define this term, the subsequent sections list the various types of plated-through holes and the various demands on the filling material related thereto.

2.1 Different types of plated-through holes

There are three types of vias:

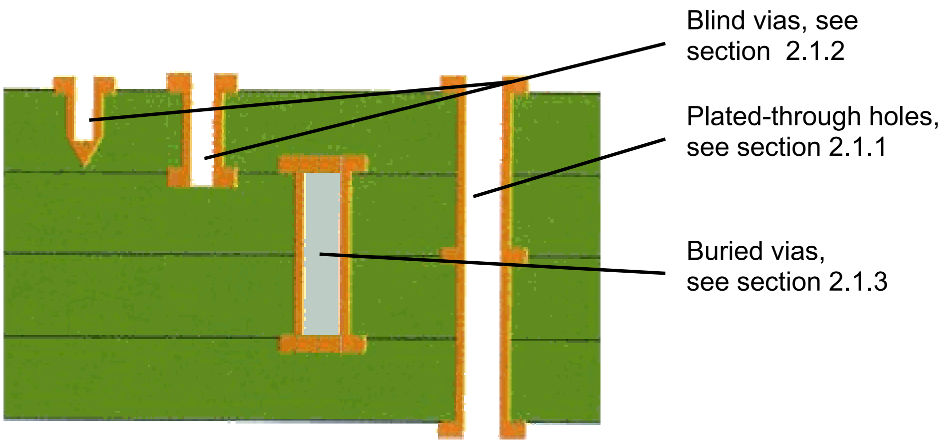

Fig. 1: Types of vias

2.1.1 Plated-through holes (PTH's)

Plated-through holes are metallized holes passing through the entire pwb. These vias do not require a planar, complete filling as no sequential layers are built-up.

In this case the "classical“ **via hole filler SD 2361** is used. It serves the purpose of filling the via hole in order to prevent solder from passing to the component side and also of ensuring the sealing for vacuum adaptation in the in-circuit test as well as of preventing flux agent residues from settling in the vias and form microclimates in these or underneath components.

Demands on the via hole filler:

- solvent-free or solids content of 100% to avoid volume shrinkage and solvent inclusions
- resistance to process chemicals
- resistance to Hot-Air Levelling processes.

2.1.2 Blind Vias

Another form of vias are the so-called blind vias. They provide the interconnection of the sequentially built-up layers as well as to the core.

During lamination of the next layer air inclusions may occur that would lead to cracks in the pwb in case of later thermal stress. In case of resin-coated foils, extensive filling is achieved by using the laminate resin. However, this is not filled and may lead to cracking in case of thermal shock loads owing to the substantial expansion in the direction of the z-axis.

The plugging of blind vias turns out to be very difficult because in this process air inclusions can hardly be avoided. Trials with the **plugging paste PP 2795-SD**, that were performed in a modified screen printing process under vacuum, however, yielded initial promising results.

The use of liquid epoxy dielectrics that enable the flow-filling of the vias without air inclusions is a possible alternative since suitable filling materials can effect lower coefficients of thermal expansion of the dielectrics. However, neither any appropriate processes nor products exist yet.

2.1.3 Buried vias

The third sort of vias which are the subject of the subsequent "plugging process" are **buried vias**. These plated-through holes pass through the entire inner layer core of a multilayer and are covered by the sequential build-up layers. They differ from blind vias in that in the beginning they are "open" and can thus be more easily filled as regards the avoidance of air inclusions, because filling is effected from one side and the air can escape on the other.

2.2 Microvias

According to the Institute for Interconnecting and Packaging Electronic Circuits (IPC) microvias are defined as vias with a diameter of < 150 µm.

The smaller, lighter and flatter end units (e.g. mobile telephones) that are required by the end users force circuit developing companies to package more circuits in a small space. In this context, microvia technology offers the advantage of saving space owing to a small diameter of the via and thus smaller pad geometries. The simultaneous possibility of doing without the connection fan-out by means of direct wiring via the SMD pads (µVIP – micro via in pad) offers even more advantages because the outer wiring is not disturbed by the plated-through holes (PTH's).

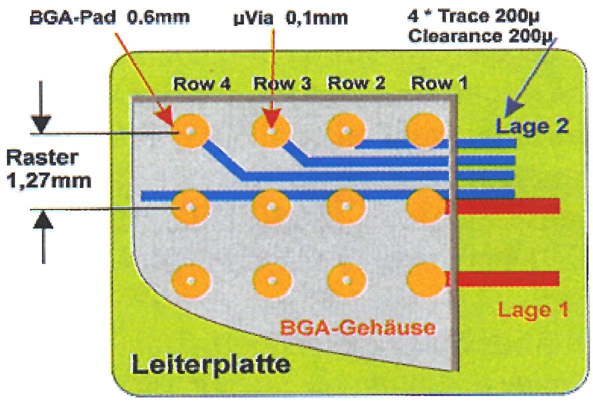

Fig. 2: Example of a pwb with microvias

3. Plugging

3.1 Why plugging?

The buried vias must be plugged completely and as level as possible in order to avoid air inclusions in the course of the sequential multilayer build-up. The structuring of the next circuit level also calls for planarity in order to avoid stray light /undercutting during exposure and the etching process.

Both sorts of dielectrics that are used worldwide for the sequential build-up of the outer layers are viscous materials such as liquid epoxy and resin-coated copper foils (**RCC**). When using liquid epoxy plugging is indispensable because the dielectric does not flow into the microvias in an adequate manner. Also compared to the use of resin-coated copper foils, with which the filling of the microvias can be effected via the resin of the copper foils, the plugging process offers decisive advantages.

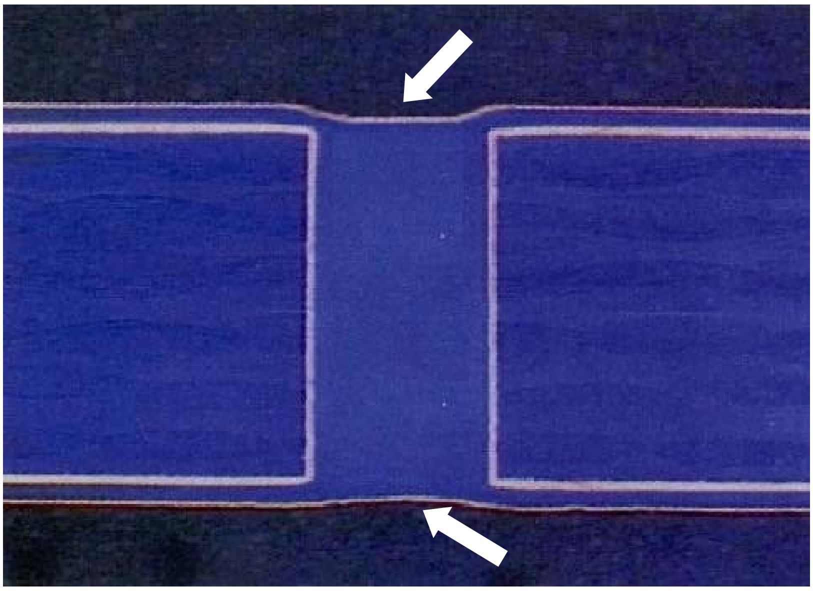

Fig 3:
cavernous surface of a microvia circuit with which
no plugging process was performed prior to foil bonding

The resin of the resin-coated copper foil has a relatively large coefficient of thermal expansion (CTE) of approx. 60 ppm below the glass transition temperature 165 °C that is typical of unfilled resin systems (RCF - by Polyclad, article in the journal "Galvanotechnik“, volume 89, issue no. 7, 1998, page 2421).

In case of thermal shock loads the occurring thermal loads are increased by the thermal expansion of the air inclusion in the vias owing to the different coefficients of thermal expansion (CTE) of the combined materials; this results in delaminations or cracking. In case of thermal shocks these cracks may lead to failures.
The filling of larger via volumes, for instance with thicker boards, leads to cavernous indentations in the copper layer because sufficient resin material cannot flow in (see fig. 3).

The **plugging paste PP 2795** was especially developed for of filling multilayer buried vias. The 100% solids content and a specially correlated filler combination ensure a low coefficient of thermal expansion of < 40 ppm so that no cracking or delamination will occur in case of thermal shock.

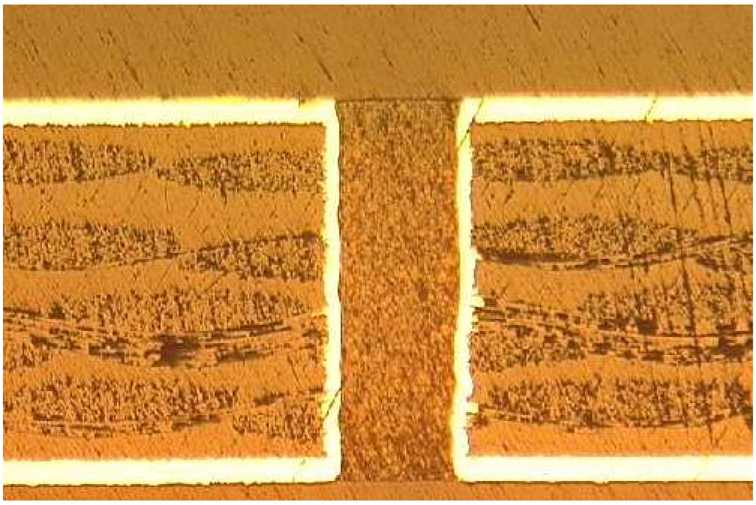

Fig. 4: highly planar surface of a microvia circuit after the brushing process

If required by the process, the planarized plugging paste can also be metallized in the usual procedure. Buried vias that are copper-plated in such a manner (fig. 5) enable a higher wiring density in the next level as well as the use of the so-called "via in pad" technology (see section 2.2 "Microvias")

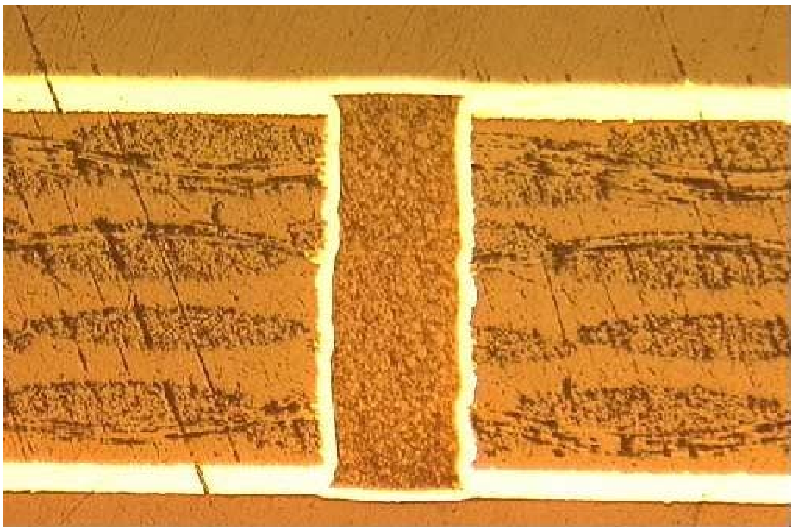

Fig. 5: highly planar surface of a microvia circuit with subsequent metallizing by the plugging process prior to applying the next layer dielectric

3.2 The plugging process

As a rule, the following production steps are observed for the optimum plugging of buried vias (see fig. 6):

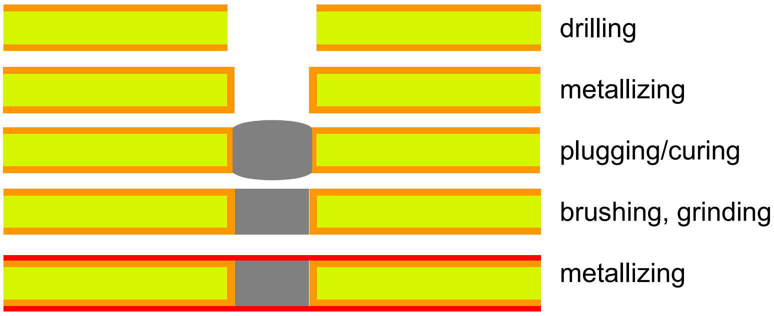

fig. 6: process flow when applying the plugging paste

Generally there are three processes available to plug buried vias at the present time:

1. Stencil printing process
2. Modified stencil printing process (Fulfill™ – Hole Fill Process)
3. Roller-coating process

All three processes are based on non-structured, plane copper-plated pwb cores.

3.2.1 Plugging by means of stencil printing

When plugging by means of the stencil printing process with the **plugging paste PP 2795-SD** (Index SD = screen printing) the vias are filled by means of a corresponding stencil. Placing a stencil that was drilled with the same drilling pattern but with larger diameters underneath the pwb has a favourable effect (see also fig. 7). The paste should be printed in such a manner that a small "hump" (nail head) remains on the underside in order to ensure a complete filling. The printing parameters largely depend upon to the "aspect ratio" of the vias (the ratio of material thickness to hole diameter) and have to be determined by means of trials. An aspect ratio of 12 can be realized with the **plugging paste PP 2795-SD**.

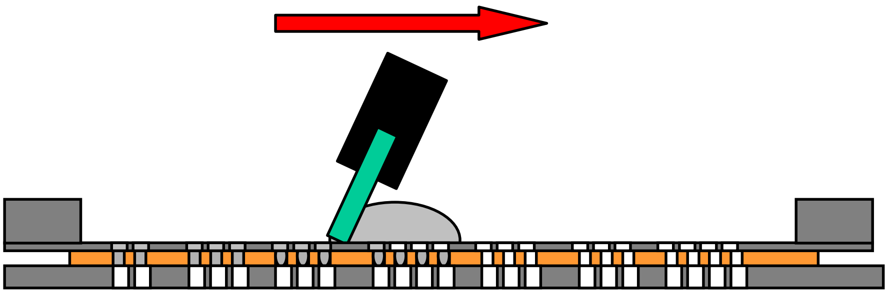

fig. 7: plugging by means of stencil printing

Printing stencil:	The stencil is stuck on V2 steel fabric, then the fabric is removed in the printing area. The stencil holes should be minimally larger than the vias of the plated-through holes.
Printing underlay:	For instance, base material where the vias are considerably larger than the diameter of the plated-through holes.
Set-up:	Only possible by pinning the reference holes.
Print:	Minimum snap-off without any lift Squeegee speed 2.0 m/min
Printing squeegee:	75 Shore / 72°
Squeegee profile:	45°, slightly broken
Flooding:	Must be well filled
Flood squeegee:	75 Shore (no metal)
Squeegee profile:	90°, sharp

Advantages of this process:

- selective plugging, i.e. only those vias are filled that need to be filled (positioning holes can be kept free)
- stencil printing is a well-known process
- the equipment already exists.

Disadvantages:

- a printing stencil is required for each layout
- difficult printing in case of substantially varying hole diameters on the pwb.

3.2.2 Modified stencil printing process (Fulfill™ – Hole Fill Process)

The Fulfill™ – Hole Fill Process is a process for filling vias with a high aspect ratio developed by Honeywell Advanced Circuits (HAC). This process is largely similar to a screen printing process but the squeegee is replaced by a "trough" via which the plugging paste is pressed into the vias. This process is set-up with a Seria screen printing machine. The main advantages of this process are as follows:

- very fast process on account of bi-directional filling
- positioning holes are exempted from filling
- suitable for an aspect ratio up to 13
- closed system prevents air from getting into the paste.

Disadvantages:

- not suitable to plug "blind via holes“ (risk of air inclusions)
- partly suitable for partial plugging of pwbs
- not suitable to plug structured pwbs
- a printing stencil (for placing underneath) is necessary for each layout.

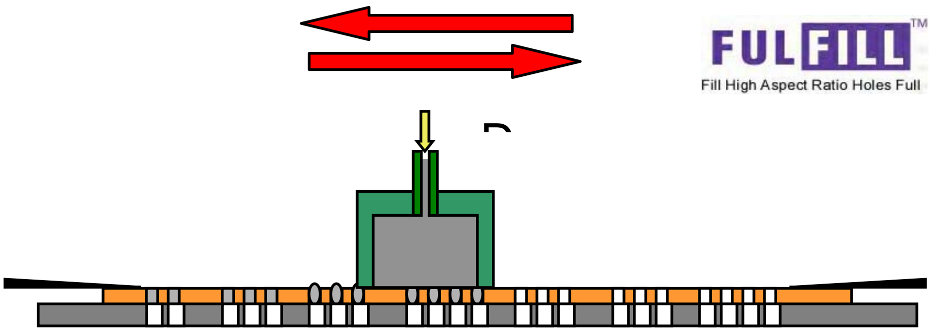

fig. 8: plugging by means of the Fulfill™ – Hole Fill Process

fig. 9: plugging results of the Fulfill™ – Hole Fill Process

3.2.3 Plugging by means of roller coating

Plugging by means of the roller coating process is effected by forcing the paste on a roller through the vias. The **plugging paste PP 2795** that was especially developed for this application method is kept in a trough while the roller coater picks up the paste on its underside. The board is pressed against the roller coater from above and the paste that is located between roller and pwb is pressed through the vias. Then the board passes between two stripper squeegees so that the plugging paste residues are removed from the board. In order to realize a slight nail head (hump) on both sides it is proven practice to position the stripping squeegees as flat as possible and slightly offset. The angle between squeegee and pwb should be < 45 ° (see fig. 10).

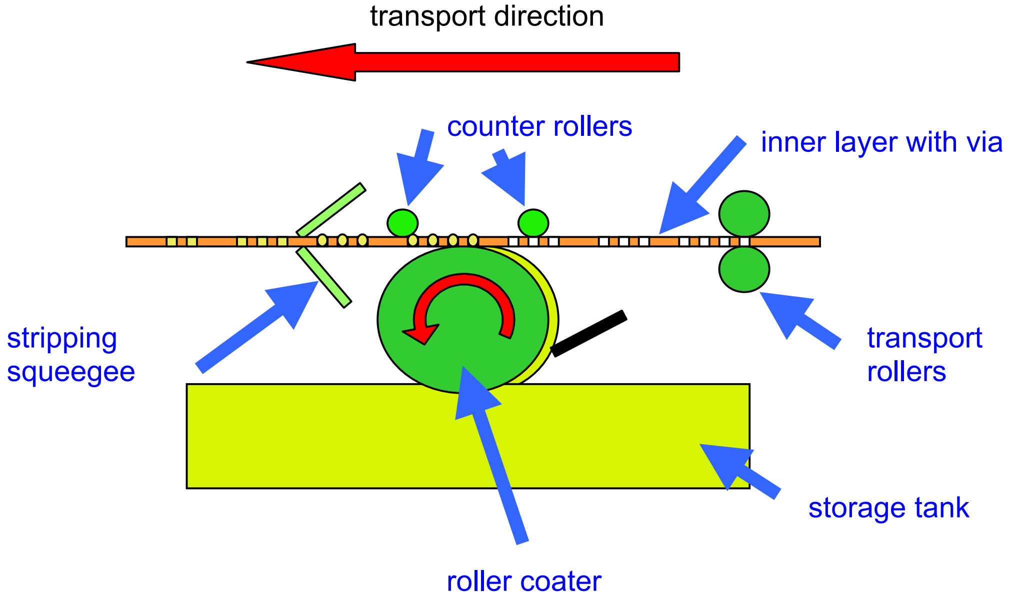

fig. 10: plugging by means of roller coating

Advantages:

- fast, secure filling of all vias
- simple process, only a few parameters have to be adjusted
- no screen stencils are required → independent of layout
- less smearing and residues on the pwb
- depending upon the stripping squeegee setting, a slight dip (plugging paste sink-in) or a slight hump (nail head) can be realized
- with PP 2795 an aspect ratio of up to 17 can be realized.

Disadvantages:

- vias that are not to be plugged have to be masked
- cannot be used for structured pwbs because the squeegees cannot remove excess material from between the conductors
- only suitable for plugging materials that have a good storage stability at room temperature because the roller coater trough capacity is 8 - 10 kg.

3.3 Thermal curing and planarization of the plugging paste

After thermal curing of the plugging paste at 150 °C for 45 min, smearing and residues of the plugging paste are removed from the pwb by means of brushing and polishing and the pwb as well as the via fillings levelled.

This process involves some critical aspects. For instance, attention must be paid to the fact that the edges of the copper barrels are not removed. Moreover, it has to be ensured that the plugging paste is not partially removed from the vias.

Practical experience shows that hard brushes with a ceramic surface give very good results in order to ensure a reproducible and perfectly even surface and avoid the problems described when planarizing. Upon request we will gladly provide you with contact addresses of reliable manufacturers of such units.

Furthermore, vertical belt grinding machines from the metal-working industry as well as oscillating grinders have stood the test.

In order to facilitate the brushing process, various adjustments of the plugging paste are available such as **FP 201-0219 UV**, that can be cured in two stages. In the first stage, the material is cured by UV radiation. The plugging paste that is still brushed easily in this stage is thermally cross-linked after levelling and thus achieves the ultimate properties desired.

3.4 Properties of the plugging pastes PP 2795 and PP 2795-SD

- 1-pack systems
- no air inclusions
- no shrinkage after curing, 100% solids content
- good adhesion between copper and plugging paste even under thermal stress (common test method 1000 cycles - 55/125 °C)
- easy brushing without any risk of a cavernous or dipped surface
- good adhesion to plated-up copper
- good adhesion of the dielectric and photo resist
- Tg > 140 °C
- CTE < 50 ppm (below Tg)
- good resistance in soldering processes; after 10 cycles at 288 °C for 10 seconds, no cracking or delamination.

3.5 Approvals for the plugging pastes PP 2795 and PP 2795-SD

The plugging pastes **PP 2795-SD** and **PP 2795** are approved according to the best flame class V-0 per UL 94 (Approbation No. File E 80315, registered trademark of ® Underwriters Laboratories Inc.; Northbrook, Illinois 60062).

Moreover, the plugging pastes of the series **PP 2795** are also certified for spacecraft applications:

Both the plugging paste **PP 2795-SD** for screen printing as well as the plugging paste **PP 2795** for roller coater application passed the **Outgassing-Test** acc. to ASTM E595.

The **NASA** (**N**ational **A**eronautics and **S**pace **A**dministration) approved test method specifies the measurement of two parameters:

- total mass loss (% TML)
- collected volatile condensate materials (% CVCM).

These two measured variables are decisive for the use of products in a vacuum. Outgassing materials can condense on sensitive electronic components and thus lead to problems/failures.

The contracted test institute **Trace Laboratories-East** confirms that our two products fulfil the substantial test criteria: The measured values are much lower than the limit values of 1.00 % for TML and 0.10 % for CVCM specified for most applications.

Thus the plugging pastes of the series **PP 2795** are the ideal product for use in space electronics. They belong to the plugging pastes approved by the NASA Jet Propulsion Laboratory.

Upon request we will gladly provide you with the full test report of Trace Laboratories-East.

3.6 Activating the plugging pastes PP 2795 and PP 2795-SD for metallization

An essential step in HDI technology is the metallization of the plugged vias. For this step, standard metallizing processes in pwb technology are used that are known from drilled-hole copper-plating. Prior to electroless copper deposition, a desmear step is required that ensures the cleaning and activation of the resin matrix. The desmear process follows this scheme:

- swelling of the resin matrix
- etching and roughening of the surface
- reduction.

The following SEM photographs show the surface before and after the desmear process.

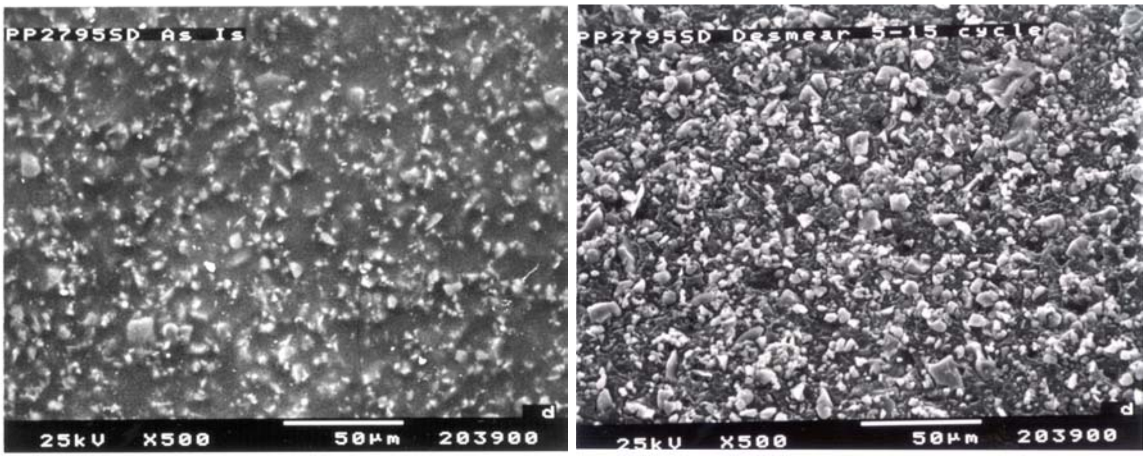

fig. 11: SEM photographs of the surface of PP 2795-SD
before and **after** the desmear process (5-15 min cycle)

The topography after the desmear process is obviously improved for electroless copper plating. Prior to the subsequent electro-copper plating, a drying step of about 60 min at 120 °C is required (detailed process information can be provided upon request).

4. Further products

The range of via hole fillers is completed by the temporary via hole fillers. These via hole fillers serve the purpose of protecting the via holes during the etching process for image generation.

The temporary via hole filler **FP 200-0128 UV** is UV-curable, etch- and plating-resistant and subsequently alkaline-strippable.

5. Contract coaters for the plugging process

Several companies are already performing contract coating with our plugging pastes. Upon request we will gladly provide you with contact addresses of such companies.

6. Technical reports

"Technical Reports" (TR) or "Preliminary Reports" (PR) from which product-specific information regarding application, processing and properties can be taken are available for all products mentioned in this **TI 15/15**. Upon request we will gladly provide you with these technical publications.

7. Literature

Regarding the subject of "HDI technology“ the following additional literature is available:

7.1 "The European technology and trend report 2001/2002 on High Density Interconnected PWBs (HDI)“, German/English
available from:
GMM – VDE/VDI-Gesellschaft Mikroelektronik, Mikro- und Feinwerktechnik
Stresemannallee 15, 60596 Frankfurt/Main, Germany
Fax: +49-69-63 12 925, E-Mail: gmm@vde.com

7.2 "Electronic assemblies - Assembly and production technology“
GMM technical report no. 37
ISBN 3-8007-2668-8
ISSN 1432-3419
available from:
VDE Verlag GmbH
Postfach 12 01 43, 10591 Berlin, Germany
Phone: +49-30-34 80 01 – 0, Fax: +49-30-34 17 093
E-Mail: vertrieb@vde-verlag.de, Internet: www.vde-verlag.de

7.3 Report no. 153 E: "Via Hole Filling and Plugging – Trends, Possibilities and Limitations for Conventional and SBU-type Fillers“
Sven Kramer and Manfred Suppa, IPC Printed Circuit Expo 2001.

7.4 Report no. 154: "Via Hole Plugging of SBU assemblies – Trends, Possibilities, Processing and Treatment as well as Limitations“
Manfred Suppa , DVS/GMM-Tagung "Elektronische Baugruppen – Aufbau und Fertigungstechnik“, February 6 - 7, 2002, Fellbach

Upon request we will gladly provide you with our reports 153 and 154. A list of further technical publications available can be found in **TI 15/101 E** (technical papers) and **TI 15/100 E** (technical information sheets).

In our report manual these technical information sheets (TI's) are filed under group 15. Or visit our web site at **http://www.peters.de**.

7.5 „A Review Of Filling High Density, High Aspect Ratio Vias In A High Volume Printed Circuit Board Industry“
Jess L. Pedigo, Mike Kittelson, Honeywell Advanced Circuits, IPC TMRC, October 2001

Any questions?

We are prepared to assist you in solving your problems. Upon request we provide you with technical documentation and free of charge samples.

The program of our associated company, **PETERS Engineering for electronic lacquers GmbH + Co KG**, contains suitable equipment of reliable manufacturers. Upon request we will gladly submit you a corresponding offer.

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